

FIG. 1

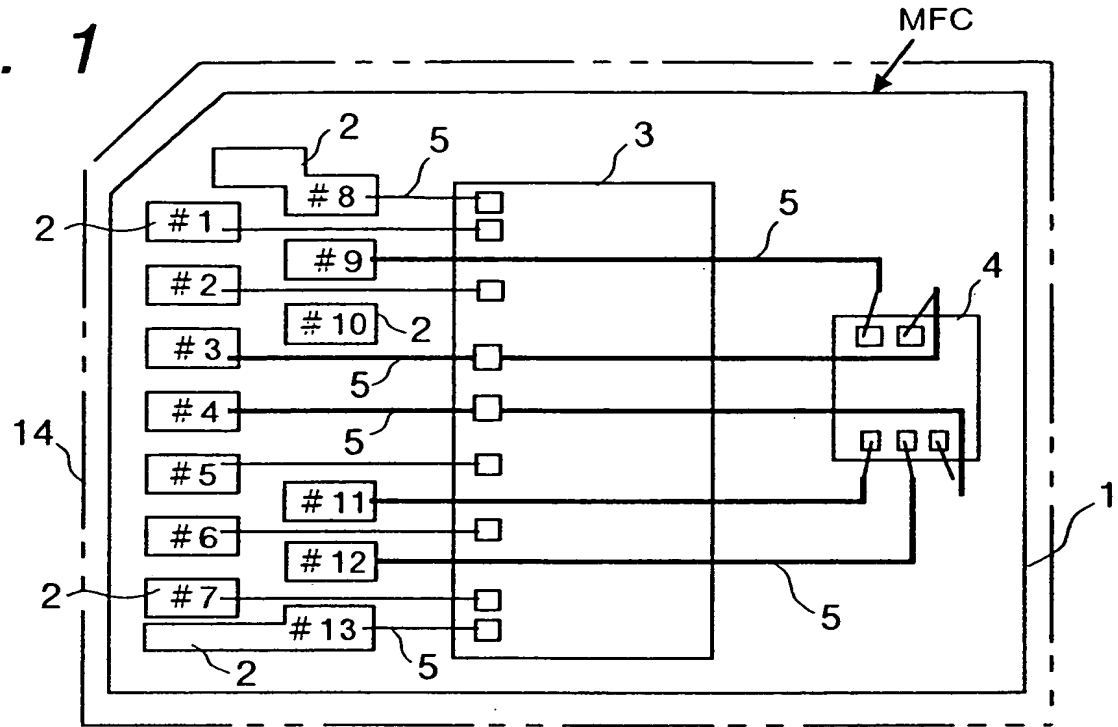


FIG. 2

pin #	7pin (1bit)	9pin (4bit)	13pin
1	(CS) NC	Data3	Data3
2	(Din) CMD	CMD	CMD
3	Vss1	Vss1	Vss1
4	Vdd	Vdd	Vdd
5	CLK	CLK	CLK
6	Vss2	Vss2	Vss2
7	(Dout) Data	Data0	Data0
8	-	Data2	Data2
9	-	-	I/O
10	-	-	NC
11	-	-	CLK
12	-	-	RST
13	-	Data1	Data1

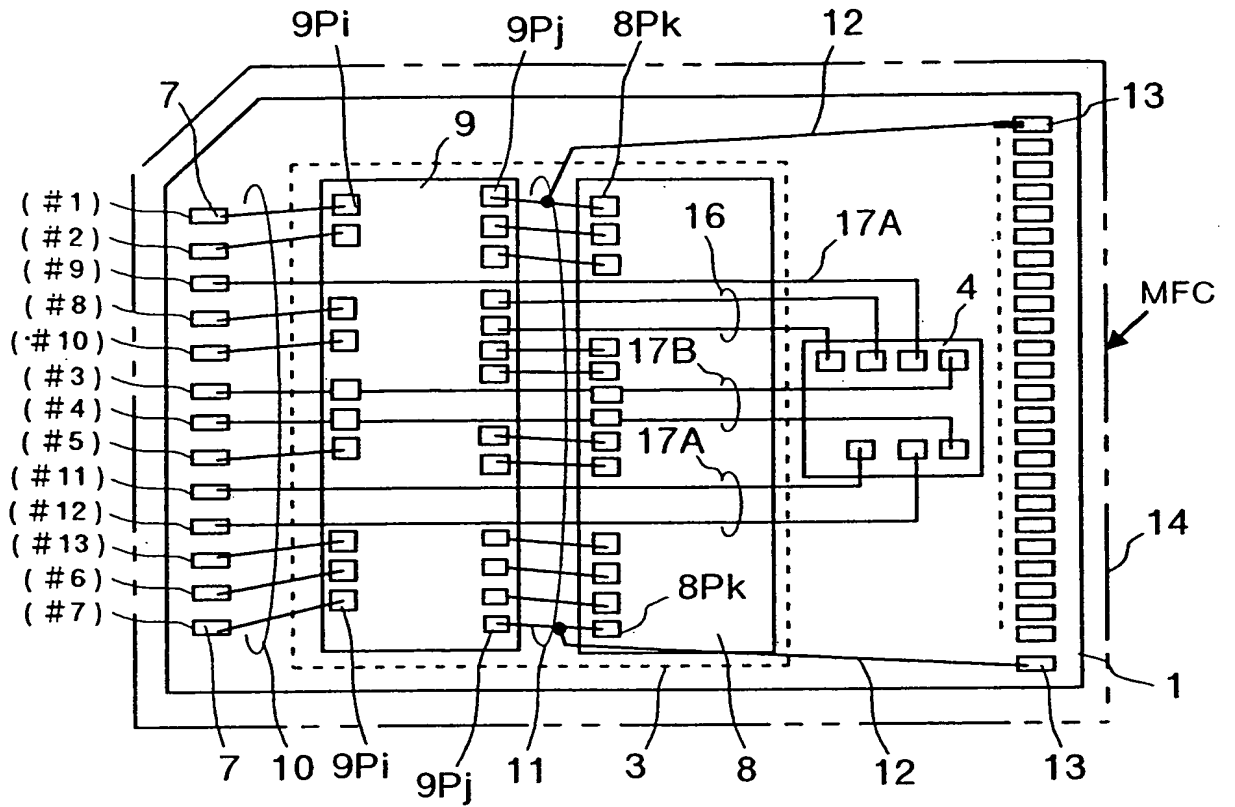
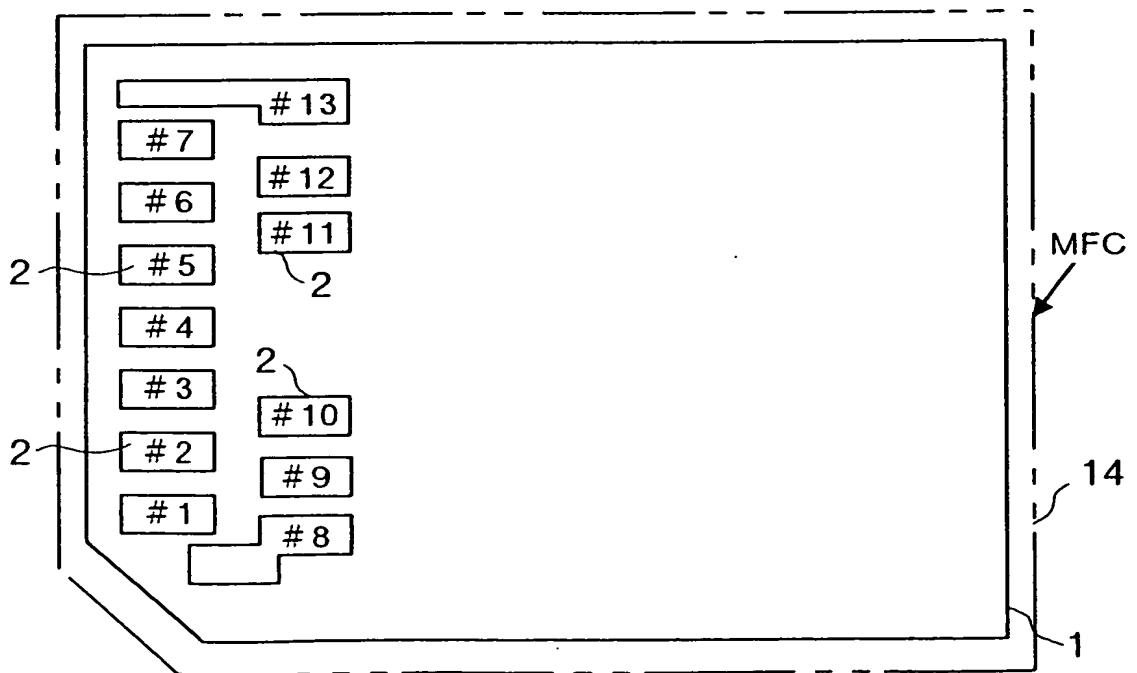
FIG. 3**FIG. 4**

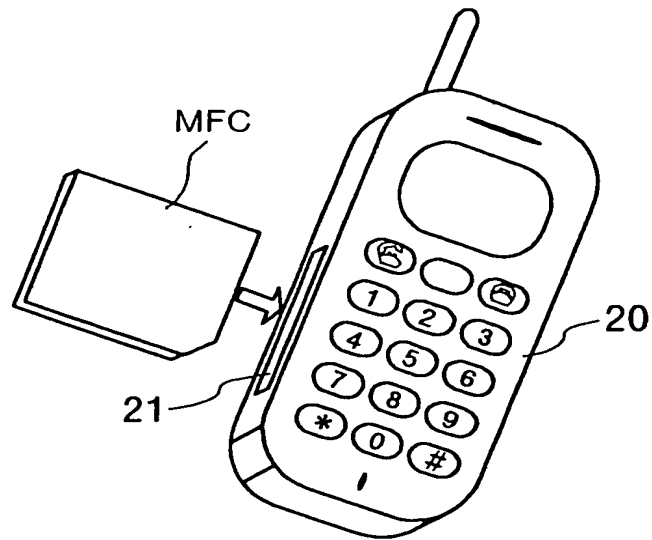
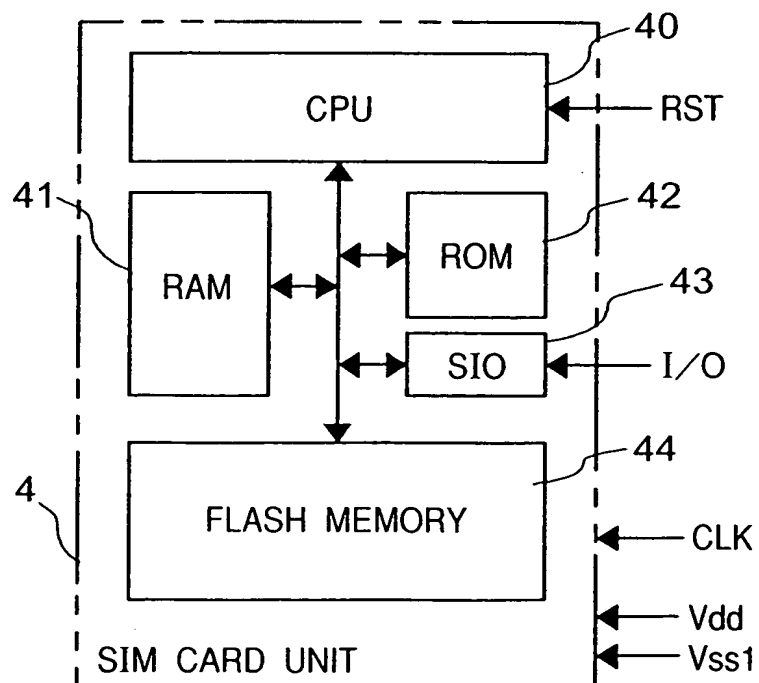
FIG. 5**FIG. 9**

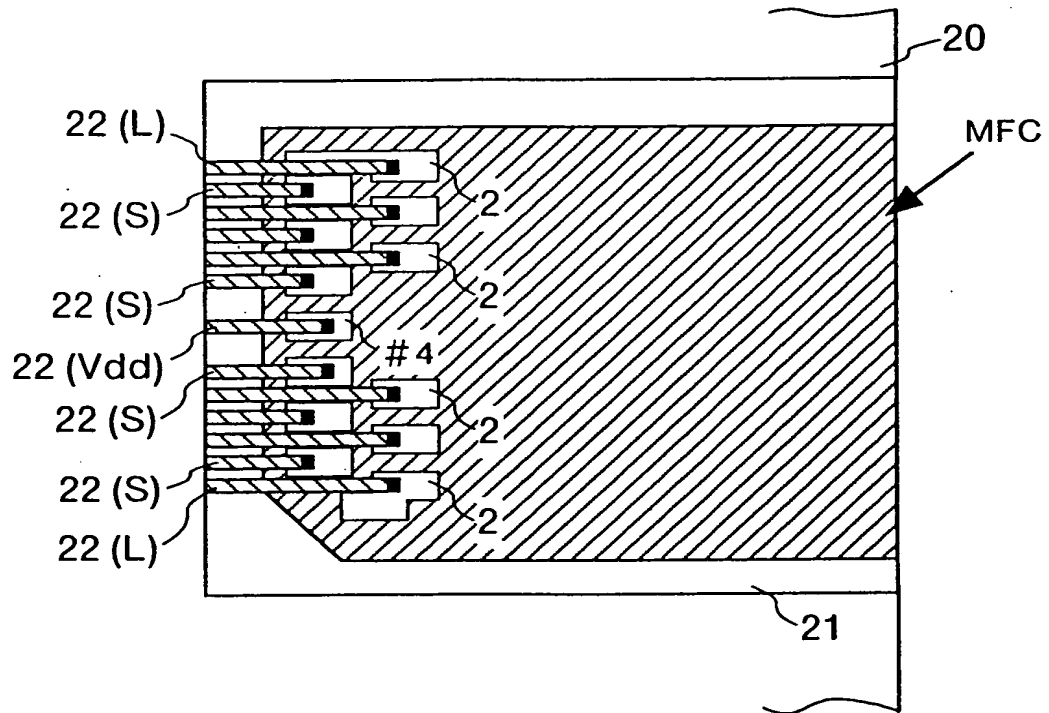
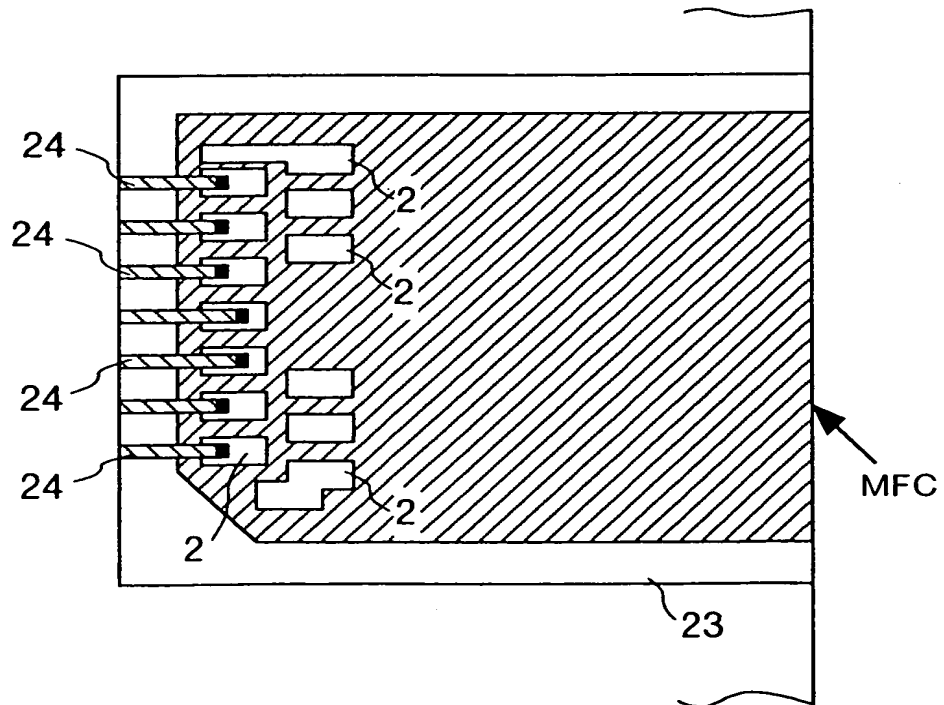
FIG. 6*FIG. 7*

FIG. 8

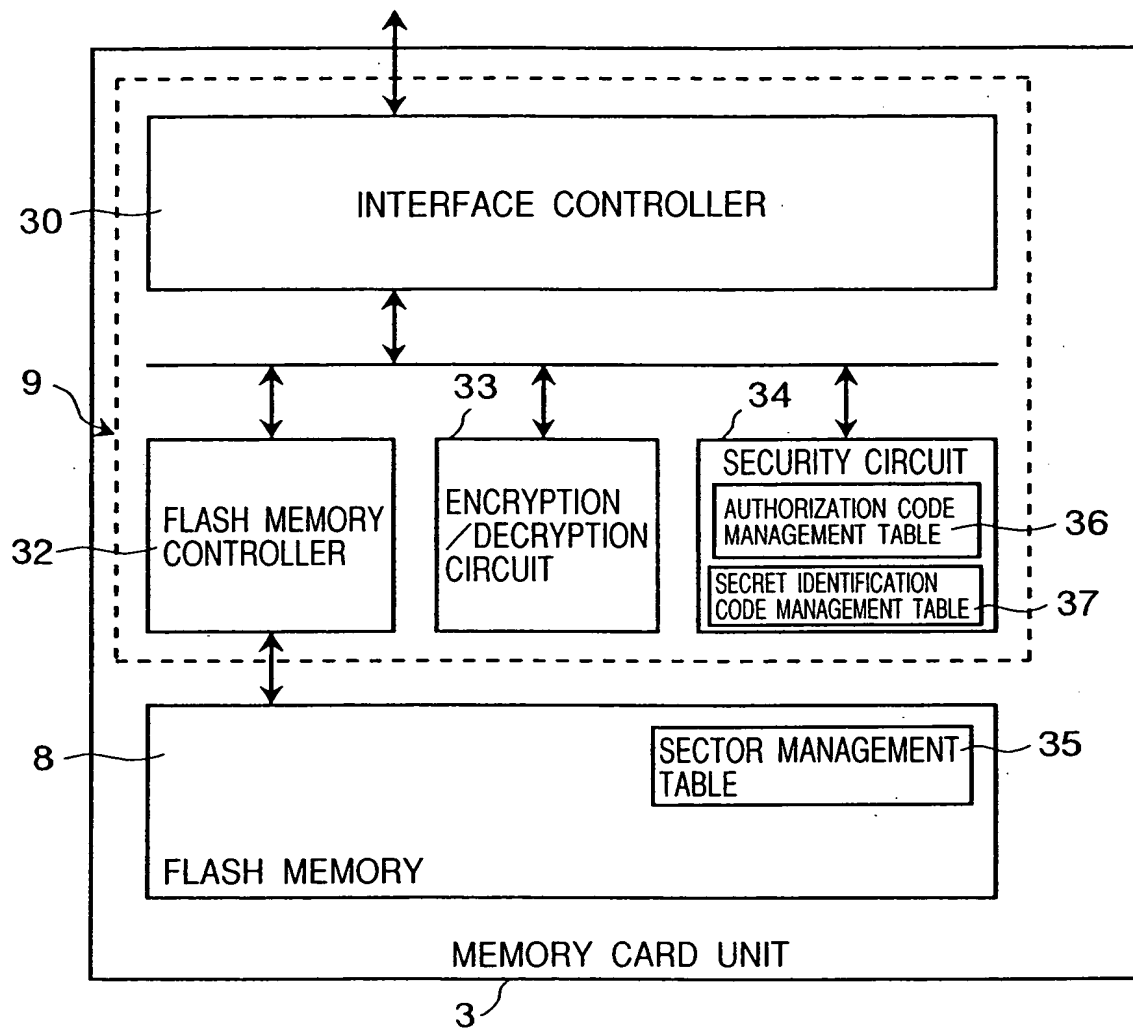


FIG. 10

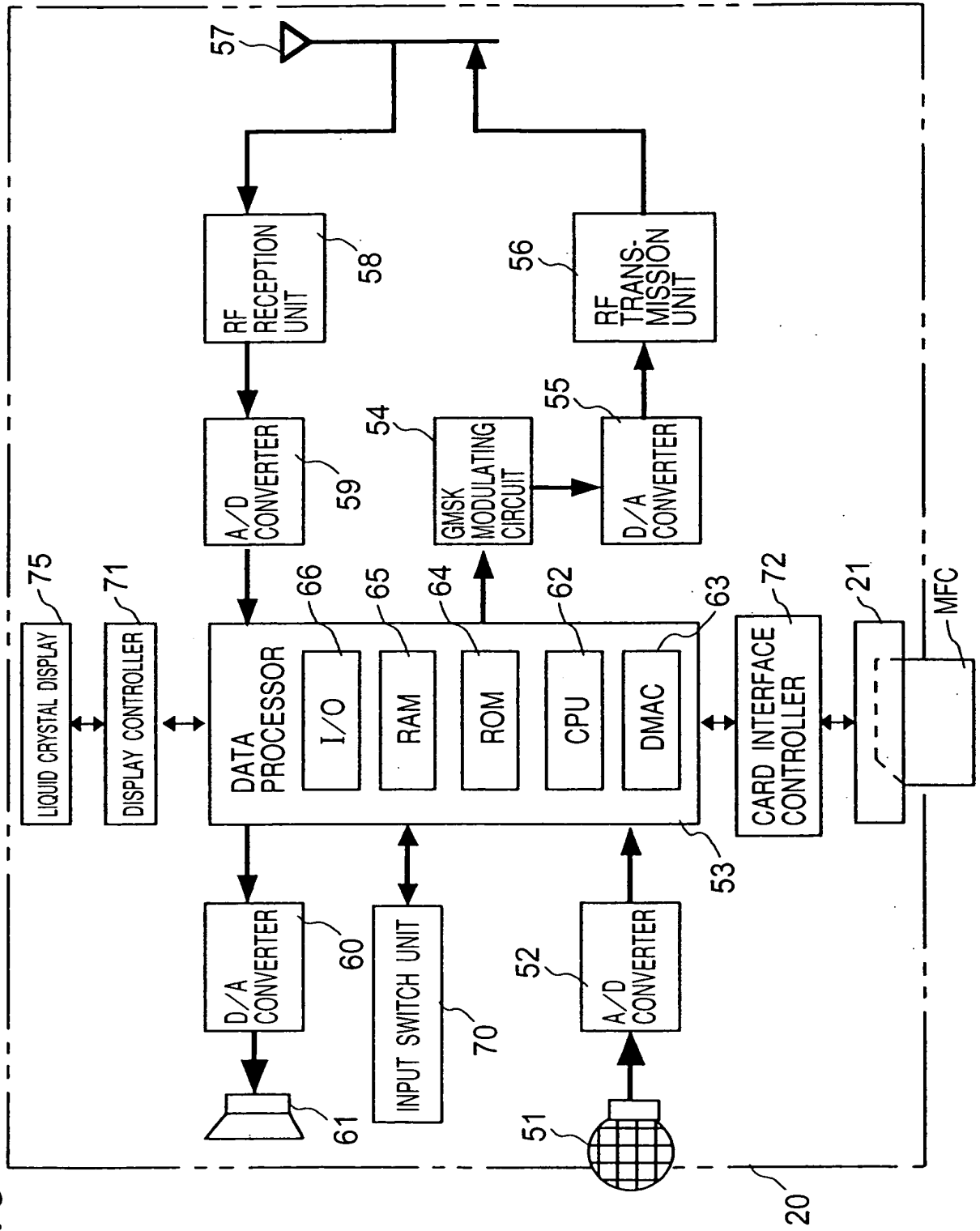
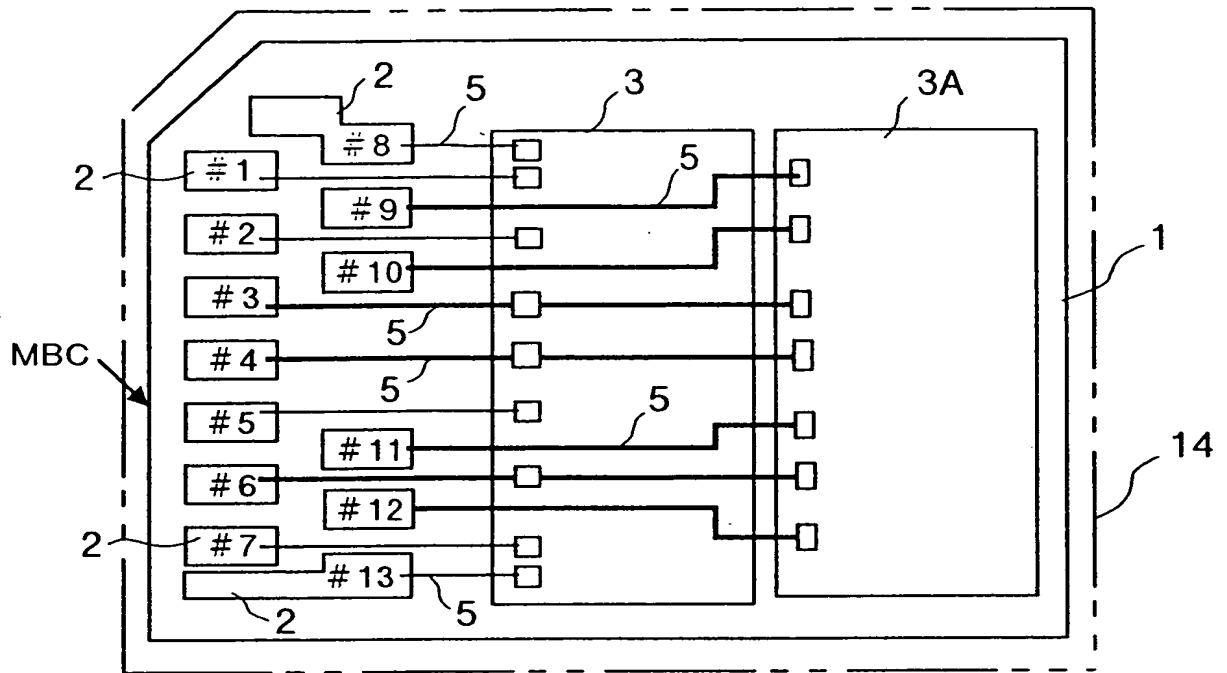


FIG. 11**FIG. 12**

pin#	7pin (1bit)	9pin (4bit)	13pin	
			(A)	(B)
1	(CS) NC	Data3	(CS-1) NC-1	Data3
2	(Din) CMD	CMD	(Din-1) CMD-1	CMD-1
3	Vss1	Vss1	Vss1	Vss1
4	Vdd	Vdd	Vdd	Vdd
5	CLK	CLK	CLK-1	CLK-1
6	Vss2	Vss2	Vss2	Vss2
7	(Dout) Data	Data0	(Dout-1) Data-1	Data0
8	-	Data2		Data2
9	-	-	(CS-2) NC-2	NC-2
10	-	-	(Din-2) CMD-2	• CMD-2
11	-	-	CLK-2	• CLK-2
12	-	-	(Dout-2) Data-2	• Data-2
13	-	Data1		Data1

FIG. 13